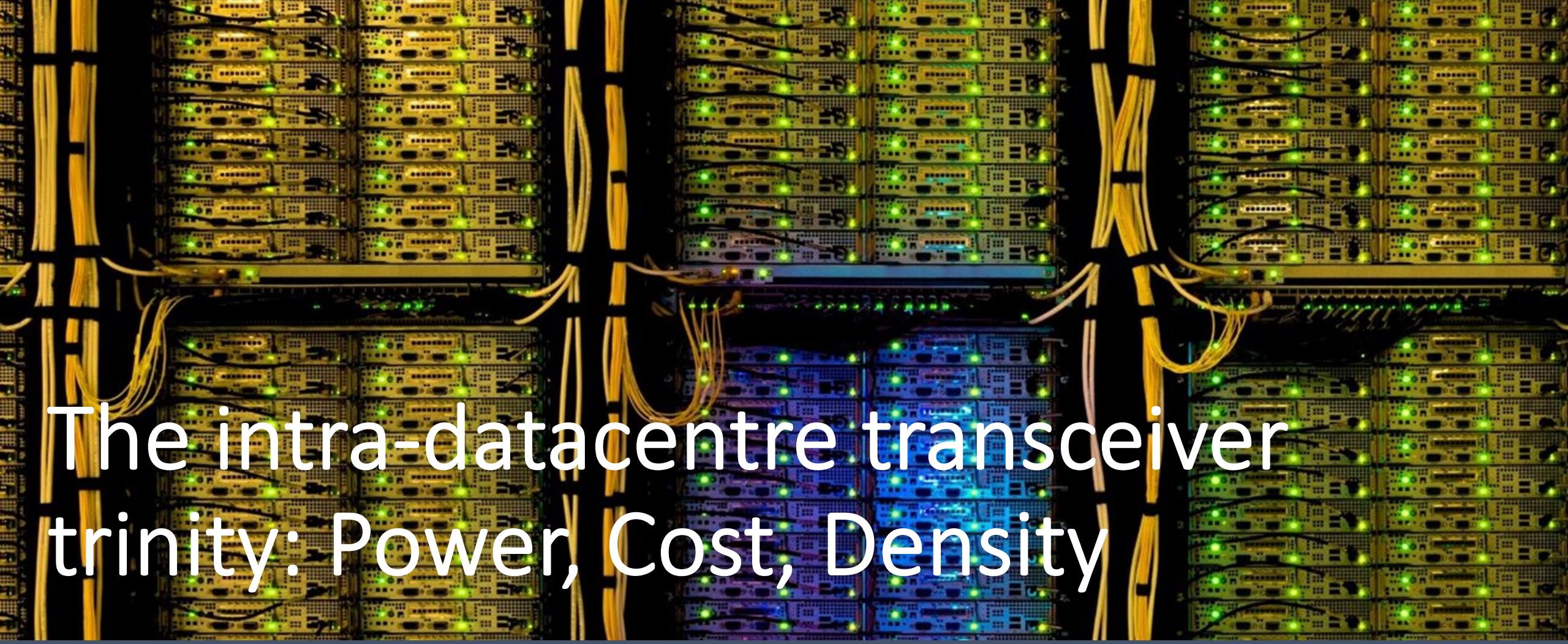


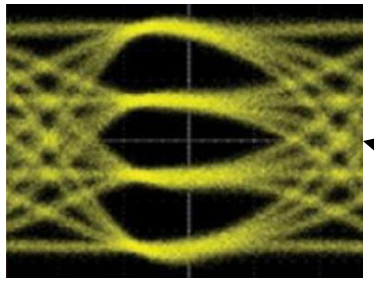
The intra-datacentre transceiver trinity: Power, Cost, Density

Benn Thomsen

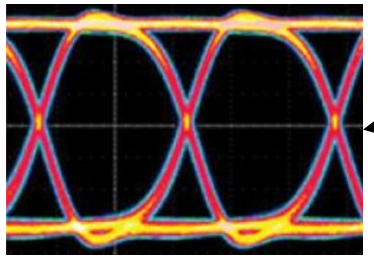
Microsoft Research

Microsoft

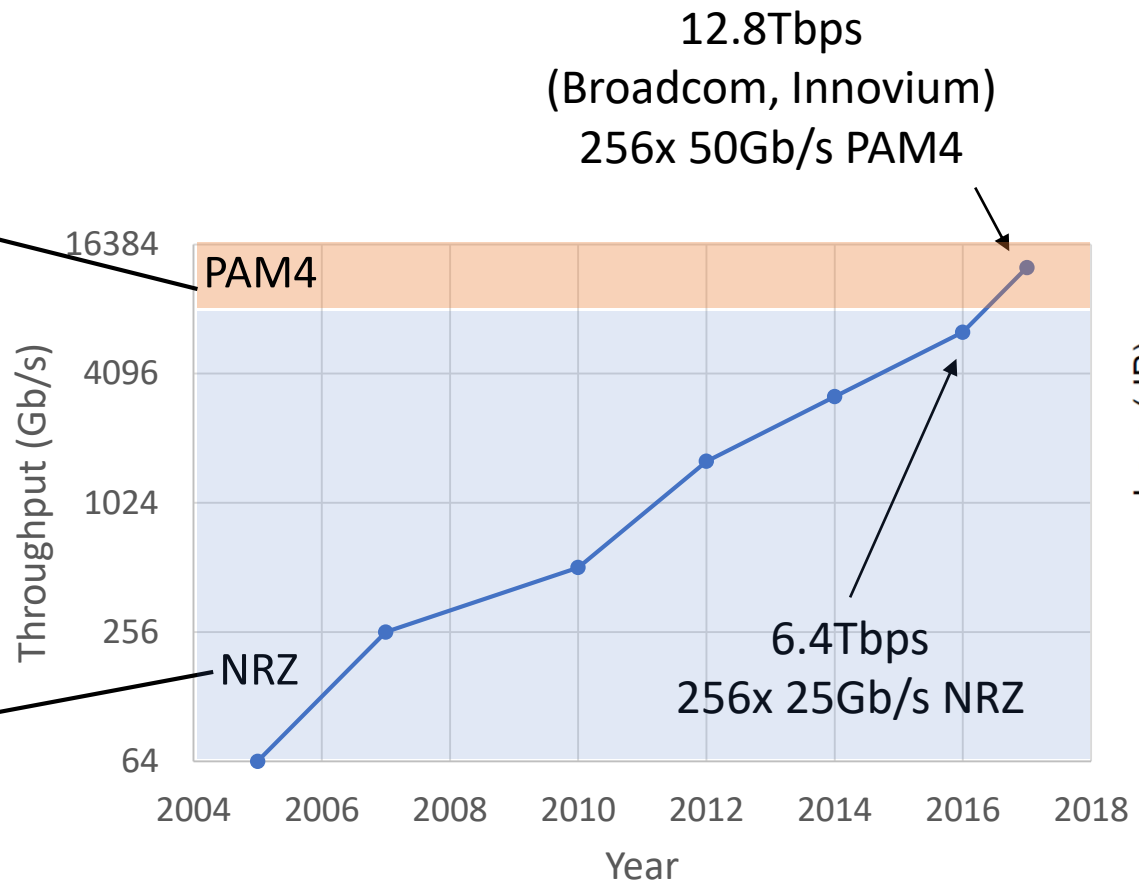
Will free switch scaling continue?



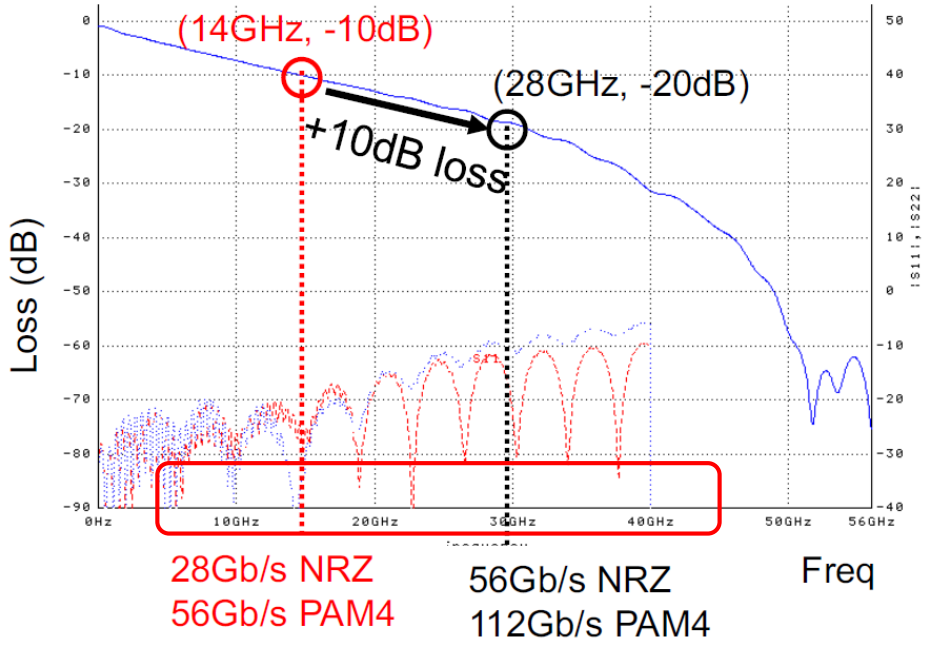
2 bits/sym

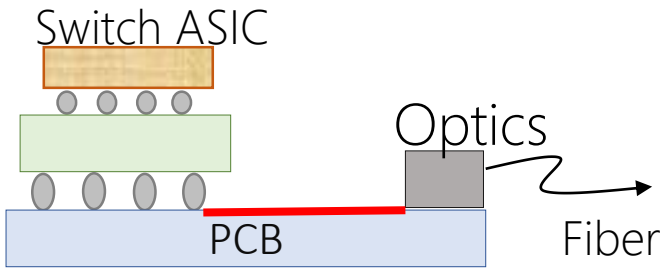


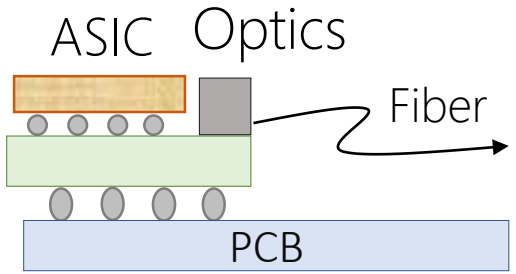
1bit/sym

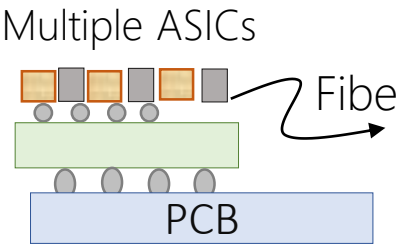


VSR Channel Loss









CMOS Scaling limit

Switch ASIC

6.4T	12.8T	25.6T	52.1T
256 x 25G	256 x 50G	256 x 100G	256 x 200G

2016 2018 2020 2022 2024 2026

SERDES

100Gbps	200Gbps	400Gbps
25Gbps NRZ	50Gbps PAM4	100Gbps PAM4
25Gbaud	25Gbaud	50Gbaud

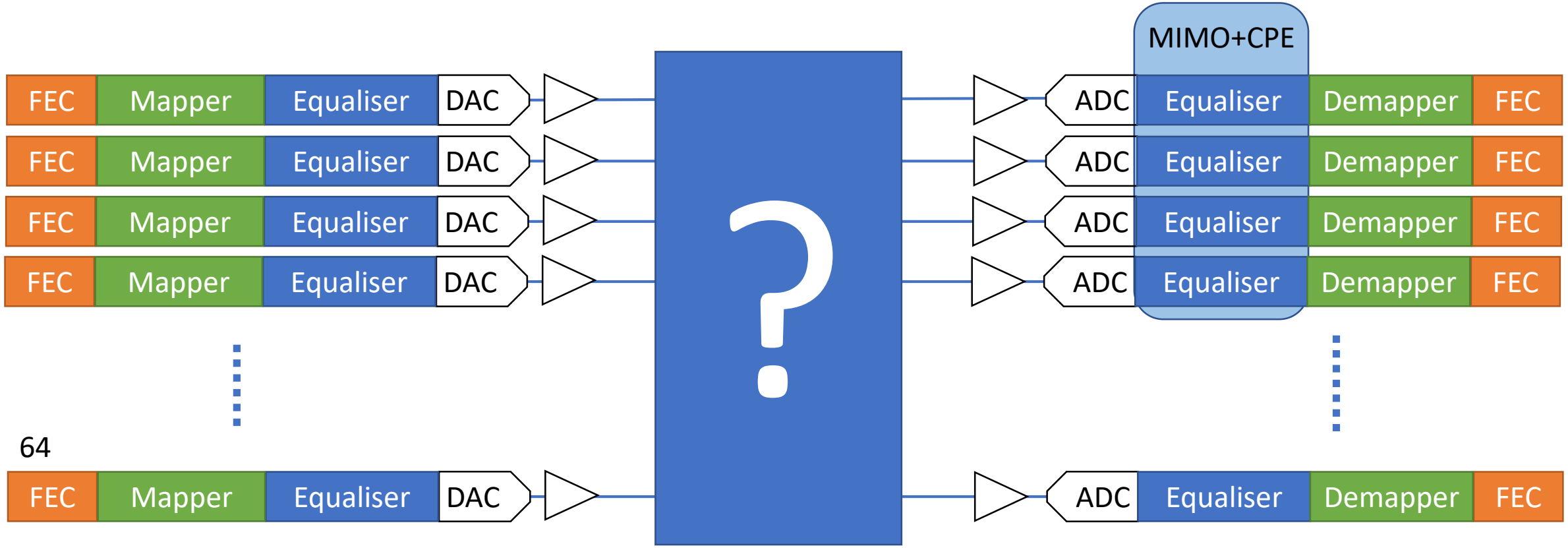
Pluggables

Stall

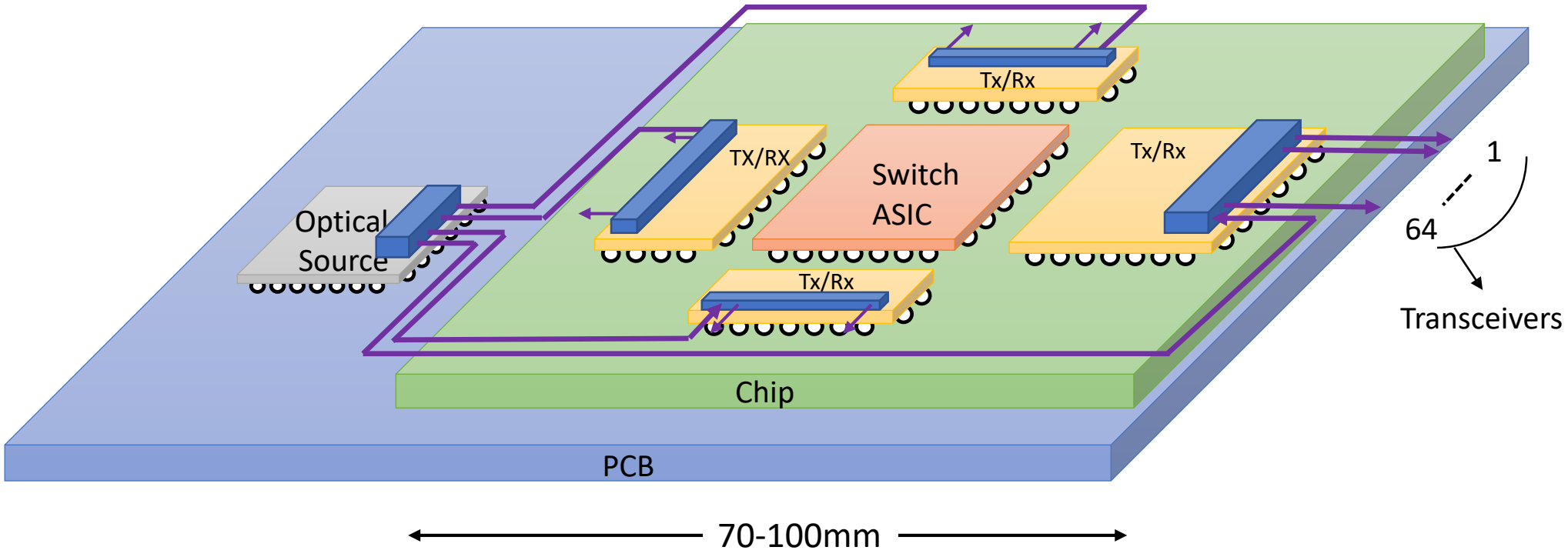
800Gbps
200Gbps PAM4
100Gbaud

In Package Optics

What will an IPO tile with 100Gbaud SerDes look like given m>2?

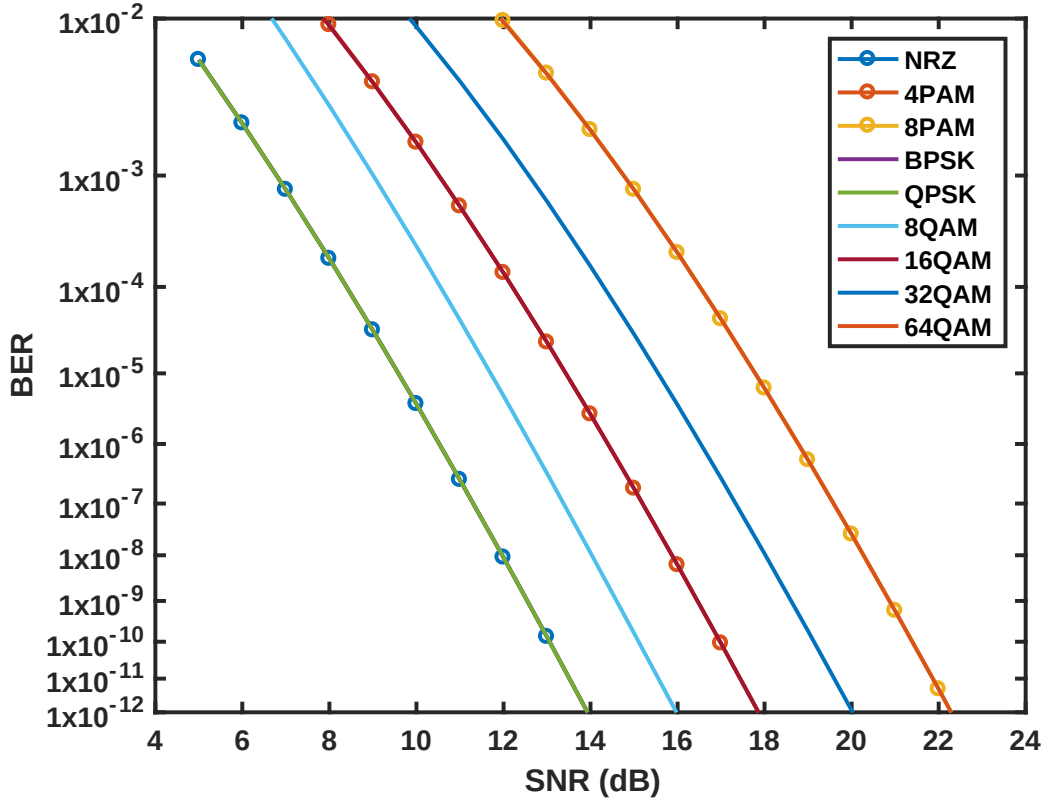


In-package optics (IPO)

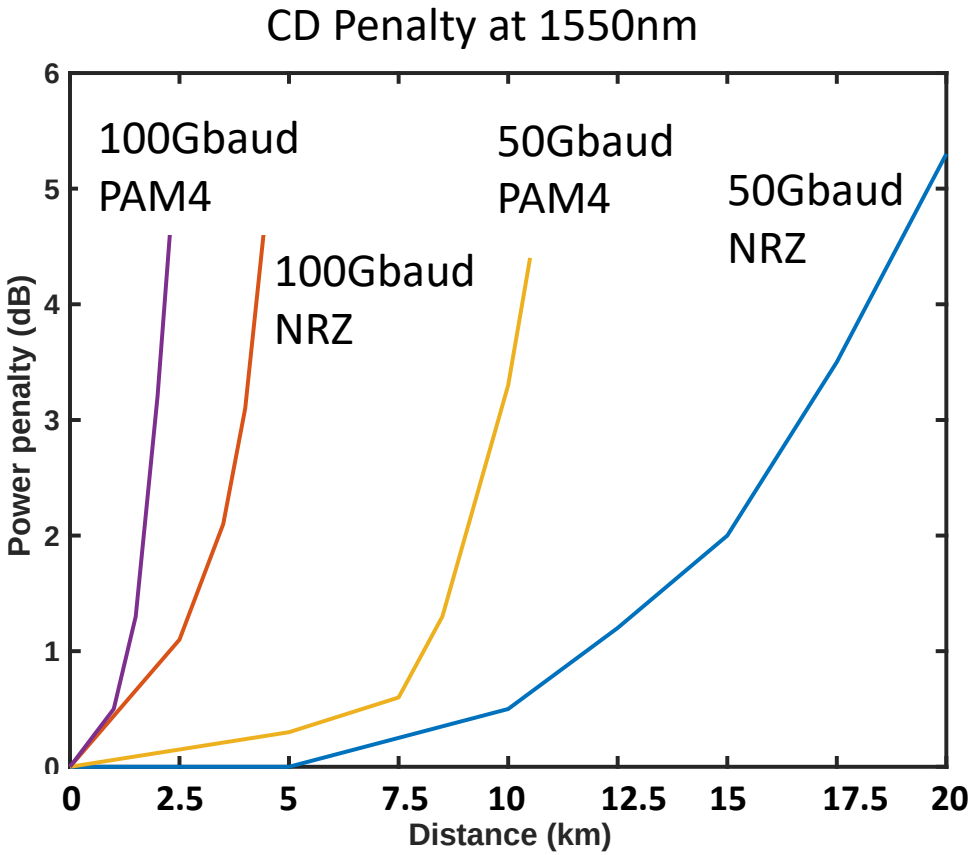


- Material
  - Silicon
    - Small waveguide size and bends
    - Requires off chip source
  - InP (yield)
- Modulator
  - Absorption or Ring Resonator based (size)
  - Performance challenges at 100GBaud
- Fibre attach ($$$$)
  - Limited chip edge real estate

Where coherent has an advantage



SNR: Use coherent link margin to reduce power hungry FEC



Overcoming channel impairments as baud rate increases

52.1T Switch with IPO