Eric S. Chung

Curriculum Vitae—March 2013

Microsoft Research
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Research Interests

- Computer architecture, energy-efficient systems, reconfigurable computing, hardware specialization
- Specialized hardware and software for big data, domain-specific languages, high-performance computing
- Hardware design automation, FPGA-based simulation methodology

Education

- **Carnegie Mellon University – Pittsburgh, PA**
  PhD in Electrical and Computer Engineering, 2011
  Thesis: "CoRAM: An In-Fabric Memory Architecture for FPGA-based Computing"
  Advisor: Prof. James C. Hoe

- **University of California Berkeley – Berkeley, CA**
  B.S. in Electrical Engineering and Computer Science, 2001—2004

Professional Experiences

- Post-doctoral Researcher, 2011-2013, *Microsoft Research SVC, Computer Architecture Group*
  Mountain View, CA, Mentor: Chuck Thacker
- Graduate Student Researcher, 2004-2011, *Carnegie Mellon University, Computer Architecture Lab*
  Pittsburgh, PA, Advisor: James C. Hoe
- Co-founder, 2008—*Meganudge Entertainment LLC,* Pittsburgh, PA
  (developed, marketed, and released a Top 25 iPhone app featured by Apple)
- Research Intern, May—2008, *Microsoft Research SVC, Computer Architecture Group*
  Mountain View, CA, Mentors: Chuck Thacker, John Davis
- Research Assistant, 2002—2004, *Group for User Interface Research at UC Berkeley*
  Berkeley, CA, Mentors: Prof. James Landay, Prof. Jason Hong, Jimmy Lin
- Co-founder, 2003—2005, *Berkeley Innovation* – Berkeley, CA

Teaching Experiences

Teaching Assistant
- 18-240: Fundamentals of Computer Engineering at CMU with Prof. James Hoe (2006, TA rating: 4.5/5.0)
- 18-741: Advanced Computer Architecture at CMU with Prof. James Hoe (2005, TA rating: 4.7/5.0)
- CS150: Design Techniques for Digital Systems at UCB with Prof. Randy Katz (2004, TA rating: 4.1/5.0)
- EE42: Intro to Digital Electronics at UCB with Prof. Andrew Neureuther (2003, TA rating: 4.8/5.0)

Students Mentored
- Jaewon Lee*, Pohang University of Science and Technology (MSR Intern, Fall 2012)
- Maysam Lavasani*, University of Texas at Austin (MSR Intern, Summer 2012)
- Srinidhi Kestur*, University of Pennsylvania (MSR Intern, Fall 2011)
- Taylor Womak, Carnegie Mellon University (ECE Intern, Summer 2011)
- Sriteja Tangeda, Carnegie Mellon University (ECE Intern, Summer 2010)

  * Jointly mentored with John Davis

Research Projects

- **CoRAM: A Scalable, Portable Memory Architecture for FPGA-based Computing (2009—Present)**
  I lead the CoRAM project, an effort to harness the capabilities of FPGAs while addressing their portability and programmability challenges [5, 6]. CoRAM exposes a portable software abstraction that greatly simplifies the management of FPGA memory and computation resources [3, 5]. Recently, we have implemented new compiler techniques that yield highly optimized implementations on existing FPGAs based on static analysis of application-specific memory behaviors [2]. The key ideas and artifacts of CoRAM are being presented and disseminated at major conference tutorials (MICRO'12, FPGA'13).

- **Specialized Hardware for Big Data (2011—Present)**
  At Microsoft Research, I initiated the LINQits project with John Davis, an effort to build composable, flexible hardware templates for accelerating data-intensive applications efficiently on mobile devices. Currently, our LINQits prototype on a heterogeneous ARM-FPGA processor achieves an order-of-magnitude energy efficiency gain relative to tuned C code [1]. We are currently developing a LINQits-aware runtime that gracefully integrates specialized hardware in the C# programming language.

- **A Low-Cost Circuit-Switched Datacenter Network (2011—Present)**
  At Microsoft Research, I am collaborating with Chuck Thacker, Andreas Nowatyzk, Tom Rodeheffer, and Fang Yu to develop a low-cost, FPGA-based circuit-switched network for the datacenter [13]. For this effort, I developed the RTL implementation of a high-radix, 128x128 circuit-switched crossbar targeting FPGAs. Along with Fang Yu, I performed a detailed cost analysis of the new network architecture— illustrating an approximately 2X cost savings relative to state-of-the-art datacenter networks.

- **ProtoFlex: FPGA-based Simulation of Full-System Multiprocessors (2005—2010)**
  At CMU, I was the lead developer of the ProtoFlex project, which investigated techniques for virtualizing the simulation of full-system multiprocessors using FPGAs. ProtoFlex was the first system of its kind to introduce *hybrid simulation* and *host interleaving techniques*, which made it practical to emulate a 16-way UltraSPARC III multiprocessor system running Oracle TPC-C on a single BEE2 FPGA platform [10]. Our subsequent work showed how FPGAs can enable *real-time instrumentation* of software without incurring a significant slowdown [8]. We have released the ProtoFlex source code and presented tutorials at major computer architecture conferences (ISCA, ASPLOS, MICRO, ISPASS, IISWC).

Journal and Fully-Reviewed Conference Publications

1. Eric S. Chung, John D. Davis, Jaewon Lee. "LINQits: Big Data on Little Clients." *International Symposium on Computer Architecture (ISCA)*, Tel-Aviv, Israel, June 2013.
2. Eric S. Chung, Michael K. Papamichael. "ShrinkWrap: Compiler-Enabled Optimization and Customization of Soft Memory Interconnects." *International Symposium on Field-Programmable Custom Computing Machines (FCCM),* Seattle, WA, April 2013.
3. Eric S. Chung, Michael K. Papamichael, Gabriel Weisz, James C. Hoe, Ken Mai. "Prototype and Evaluation of the CoRAM Memory Architecture for FPGA-Based Computing." *International Symposium on Field-Programmable Gate Arrays (FPGA),* Monterey, CA, Feb 2012.
4. Srinidhi Kestur, John D. Davis, Eric S. Chung. "Towards a Universal FPGA Matrix-Vector Multiplication Architecture." *International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Toronto, Canada, Apr 2012.
5. Eric S. Chung, James C. Hoe, Ken Mai. "CoRAM: An In-Fabric Memory Architecture for FPGA-based Computing." *International Symposium on Field-Programmable Gate Arrays (FPGA),* Monterey, CA, Feb 2011. **(Best Paper Award)**

6. <u>Eric S. Chung</u>, Peter A. Milder, James C. Hoe, Ken Mai. "Single-Chip Heterogeneous Computing: Does the Future Include Custom Logic, FPGAs, and GPGPUs?" *International Symposium on Microarchitecture (MICRO),* Atlanta, GA, Dec 2010.
7. <u>Eric S. Chung</u>, James C. Hoe. "High-Level Design and Validation of the BlueSPARC Multithreaded Processor." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol.29, no.10,* Oct 2010.
8. <u>Eric S. Chung</u>, Michael K. Papamichael, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai. "ProtoFlex: Towards Scalable, Full-System Multiprocessor Simulations Using FPGAs." *ACM Transactions on Reconfigurable Technology and Systems (TRETS), Volume 2, Issue 2,* Jun 2009.
9. <u>Eric S. Chung</u>, James C. Hoe. "Implementing a High-performance Multithreaded Microprocessor: A Case Study in High-level Design and Validation." *Formal Methods and Models for Codesign (MEMOCODE),* Cambridge, MA, Jul 2009.
10. <u>Eric S. Chung</u>, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai. "A Complexity-Effective Architecture for Accelerating Full-System Multiprocessor Simulations using FPGAs." *International Symposium on Field-Programmable Gate Arrays (FPGA),* Monterey, CA, Feb 2008.
11. Brian T. Gold, Jared C. Smolens, Jangwoo Kim, <u>Eric S. Chung</u>, Vasileios Liaskovitis, Eriko Nurvitadhi, Babak Falsafi, James C. Hoe, Andreas G. Nowatzyk. "TRUSS: Reliable, Scalable Server Architecture." *IEEE Micro, Special Issue on Reliability-Aware Microarchitectures,* Nov-Dec 2005.
12. <u>Eric S. Chung</u>, Jason I. Hong, James Lin, Madhu K. Prabaker, James A. Landay, Alan L. Liu. *"*Design Patterns for Ubiquitous Computing." *Designing Interactive Systems (DIS),* Cambridge, MA, Aug, 2004.

Manuscripts Under Review
13. <u>Eric S. Chung</u>, Andreas Nowatzyk, Tom Rodeheffer, Chuck Thacker, Fang Yu. "AN3: A Low-Cost, Circuit-Switched Datacenter Network."

Other Publications (Technical Reports, Workshops, and Posters)
Technical Reports
14. John D. Davis, <u>Eric S. Chung</u>. "SpMV: A Memory-Bound Application on the GPU Stuck Between a Rock and a Hard Place." *MSR-TR-2012-95*, Sep 2012.
15. Jangwoo Kim, Eriko Nurvitadhi, <u>Eric S. Chung</u>. "Opportunity of Hardware-based Optimistic Concurrency in OLTP." *Selected Project Reports from Advanced OS & Distributed Systems, Spring 2005. Technical report CMU-CS-05-138.*

Workshops and Posters
16. <u>Eric S. Chung</u>, Michael K. Papamichael. "Towards Automatic Customization of Interconnect and Memory in the CoRAM Abstraction (poster)." *International Symposium on Field Programmable Gate Arrays (FPGA)*, Monterey CA, Feb 2013.
17. <u>Eric S. Chung</u>, John D. Davis, Srinidhi Kestur. "An FPGA Drop-In Replacement for Universal Matrix-Vector Multiplication." *Workshop on the Intersections of Computer Architecture and Reconfigurable Logic (CARL)*, Portland, Oregon, Jun, 2012.
18. <u>Eric S. Chung</u>, James C. Hoe, Ken Mai. "Connected RAM: An In-Fabric Memory Abstraction for FPGA-Based Computing." *Workshop on the Intersections of Computer Architecture and Reconfigurable Logic (CARL),* Atlanta, GA, Dec, 2010.
19. <u>Eric S. Chung</u>, Michael K. Papamichael, James C. Hoe, Babak Falsafi, Ken Mai. "The Open-Source ProtoFlex Simulator (poster)." *Research Accelerator for Multiple Processors (RAMP),* Santa Cruz, CA, Jan 2010.
20. <u>Eric S. Chung</u>, Michael K. Papamichael, James C. Hoe, Babak Falsafi, Ken Mai. "ProtoFlex: Towards Scalable, Full-System Multiprocessor Simulations Using FPGAs (poster)." *Center for Circuit and System Solutions (C2S2) Annual Review*, 2009.

21. Michael K. Papamichael, <u>Eric S. Chung</u>, James C. Hoe, Babak Falsafi, Ken Mai. "ProtoFlex: Complexity-Effective FPGA-Accelerated Instrumentation (poster)." *Research Accelerator for Multiple Processors (RAMP Retreat)*, Palo Alto, CA, Aug 2008.
22. <u>Eric S. Chung</u>, Michael K. Papamichael, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai. "An MP Architectural Exploration Vehicle Using Complexity-Effective FPGA-accelerated Simulation (poster)." *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS),* Seattle, WA, March 2, 2008.
23. <u>Eric S. Chung</u>, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai. "Virtualized Full-System Emulation of Multiprocessors using FPGAs." *Workshop on Architecture Research Prototyping (WARP)*, June 2007.
24. <u>Eric S. Chung</u>, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai. "ProtoFlex: FPGA-Accelerated Hybrid Functional Simulator." *Workshop on NSF Next Generation Software Program (NSFNGS)*, Mar 2007.
25. <u>Eric S. Chung</u>, James C. Hoe, Babak Falsafi. "ProtoFlex: Co-Simulation for Component-wise FPGA Emulator Development." *Workshop on Architecture Research using FPGA Platforms (WARFP)*, Austin, TX, Feb 2006.

Patents
25. Eric S. Chung, John Davis. A CONFIGURABLE HARDWARE ACCELERATOR TEMPLATE FOR QUERY OPERATORS. *Application pending.*
26. Eric S. Chung, John Davis, Srinidhi Kestur. UNIVERSAL FPGA MATRIX-VECTOR MULTIPLICATION ARCHITECTURE. Appl. No. 336843.01. Filed October 5, 2012.

Presentations
27. Talk on CoRAM at Microsemi, Inc., San Jose, CA, March 15, 2012.
28. Talk on CoRAM at Xilinx, Inc., Campbell, CA, January 20, 2012.
29. Talk on CoRAM at Altera, Inc., San Jose, CA, March 3, 2011.
30. "Prototype and Evaluation of the CoRAM Memory Architecture for FPGA-Based Computing", *International Symposium on Field-Programmable Gate Arrays (FPGA),* Monterey, CA, February 23, 2012.
31. "CoRAM: An In-Fabric Memory Architecture for FPGA-Based Computing." *International Symposium on Field-Programmable Gate Arrays (FPGA)*, Monterey, CA, February 28, 2011.
32. "Single-Chip Heterogeneous Computing: Does the Future Include Custom Logic, FPGAs, and GPGPUs?" *International Symposium on Microarchitecture (MICRO)*, Atlanta, GA, December 6, 2010.
33. "CoRAM: An In-Fabric Memory Abstraction for FPGA-Based Computing." *Workshop on the Intersections of Computer Architecture and Reconfigurable Logic (CARL),* Atlanta, GA, December 5, 2010.
34. "Implementing a High-performance Multithreaded Microprocessor: A Case Study in High-level Design and Validation." *Formal Methods and Models for Codesign (MEMOCODE),* Cambridge, MA, July 14, 2009.
35. "Open Source Protoflex Simulator." *Research Accelerator for Multiple Processors (RAMP retreat)*, Austin, TX, June 25, 2009.
36. "A Complexity-Effective Architecture for Accelerating Full-System Multiprocessor Simulations Using FPGAs." *International Symposium on Field-Programmable Gate Arrays (FPGA),* Monterey, CA, Feb, 2008.
37. "Usability Challenges for RAMP2." *RAMP retreat*, Berkeley, CA, January 15, 2009.
38. "A Complexity-Effective Architecture for Accelerating Full-System Multiprocessor Simulations Using FPGAs." *Invited Talk at SUN Microsystems*, Santa Clara, CA, January 17, 2008
39. "ProtoFlex Status Update and Design Experiences." *RAMP retreat*, Berkeley, CA, January 17, 2008.
40. "Accelerating Architectural-Level Full-System Simulations Using FPGAs." *Invited talk at Microsoft Research*, Redmond, CA, October 24, 2007.
41. "Architectural Emulation on FPGAs Made Easy with Bluespec." *Bluespec Workshop*, MA, Aug, 2007.
42. "Virtualized Full-System Emulation of Multiprocessors using FPGAs." *Workshop on Architecture Research Prototyping (WARP)*, June 9, 2007.
43. "Protoflex: An FPGA-Accelerated Hybrid Functional Simulator." *RAMP retreat*, Berkeley, CA, Jan, 2007.

44. "Combining Simulators and FPGAs: An Out-of-Body Experience." *RAMP retreat*, Boston, MA, Jun, 2006.
45. "ProtoFlex: Co-Simulation for Component-wise FPGA Emulator Development." *Workshop on Architecture Research using FPGA Platforms (WARFP)*, Austin, TX, February 12, 2006.

Tutorials at Conferences

46. Eric S. Chung, Michael K. Papamichael, Gabriel Weisz. "Cross-Platform FPGA Accelerator Development Using the CoRAM Virtual Architecture and the CONNECT Network-on-Chip Generator." *Tutorial to appear at International Symposium on Field Programmable Gate Arrays (FPGA)*, February 11, 2013.
47. Eric S. Chung, Michael K. Papamichael, Gabriel Weisz. "Cross-Platform FPGA Accelerator Development Using the CoRAM Virtual Architecture and the CONNECT Network-on-Chip Generator." *Tutorial at International Symposium on Microarchitecture (MICRO)*, December 6, 2012.
48. Derek Chiou, Eric S. Chung, Michael K. Papamichael, Hari Angepat, Angshuman Parashar, Zhangi Tan. "RAMP Simulator Tutorial: Protoflex, FAST, HAsim, and RAMP-Gold." *Tutorial at International Symposium on Performance Analysis of Systems and Software (ISPASS)*, Mar, 2010.
49. Eric S. Chung, Mike Ferdman, and Michael K. Papamichael. "SimFlex and ProtoFlex." *Tutorial at International Symposium on Microarchitecture (MICRO)*, December 12, 2009.
50. Eric S. Chung, Michael K. Papamichael. "ProtoFlex: An Architectural Exploration Vehicle using FPGA-Accelerated, Full-System Multiprocessor Simulation." *Tutorial at International Symposium on Workload Characterization (2009)*, October 4, 2008.
51. Eric S. Chung, Michael K. Papamichael. "ProtoFlex Tutorial: Full-System MP Simulations Using FPGAs." *Tutorial at International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2, 2008.
52. Eric S. Chung, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, and Ken Mai. "RAMP tutorial: ProtoFlex." *Tutorial at International Symposium on Computer Architecture (ISCA)*, San Diego, CA, June 10, 2007.

Grant Writing Experiences

53. CCF-SHF: Rethinking the Architecture of FPGAs as First-Class Computing Devices (NSF; CCF-1012851; J. Hoe—PI, K. Mai—Co-PI; $1,000,000, 2010-2014)
54. CPA-CSA: Accelerating Architectural-level, Full-system Multiprocessor Simulations Using FPGAs (NSF; CCF-0811702; J. Hoe—PI, $314,000, 2008-2011)

Honors and Awards

- Best Paper Award, ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (2011)
- Microsoft Research Graduate Fellowship (2009-2010)
- John and Claire Bertucci Graduate Fellowship (2011)
- Carnegie Mellon Laboratory for Computer Systems Fellowship (2004)
- Department Honors, University of California Berkeley (2004)
- National Collegiate Inventors & Innovators Alliance Advanced E-Team Award (2004)
- Eta Kappa Nu: Berkeley Mu Chapter (2002)

Professional Services

- Program Committees: FCCM'12, FCCM'13
- Best Paper Award Committee: MICRO'12
- External reviewer: MICRO, HPCA, ASPLOS, FCCM, TRETS, CARL, CASES, HIPEAC, TPDS
- Member of IEEE Computer Society and ACM SIGARCH

Personal

- US citizen

References (alphabetical)

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