AMETHYST: Image Registration Engine for Multiframe Processing

Mohammed Shoaib, Rich Stoakley, Matt Uyttendayle, and Jie Liu

Sensing and Energy Research Group
Microsoft Research
Multiframe processing (MFP) enables advanced algorithms for image analysis

e.g., high-dynamic range (HDR) imaging, de-noising, image stabilization, de-blurring, super-resolution imaging, de-hazing, panoramic stitching, etc.

IMG SOURCES: (1) L. Zhang, CVPR ’10 (2) M. Tico, Nokia ERDC ’06, (3) A. Tomaszewska WSCG ’07
Why is it hard?

E.g., HDR Photography

Typically, serial processing → frame delays cause issues:

1. Moving objects create artifacts

2. Moving camera also creates artifacts

Frame misalignments lead to artifacts in fused image

IMG SOURCES: (1) L. Zhang, CVPR ’10 (2) NVIDIA whitepaper, MWC ’13
What are some existing solutions?

Solution 1: HDR Capture, *e.g.*, Toshiba T4K05

Solution 2: Algorithmic

Algorithmic solution is more interesting → needs **no hardware change** and scales to other applications

**IMG SOURCES:** (1) product brief T4K05 '13 (2) L. Zhang, CVPR '10
What are others doing about it?

**E.g., NVIDIA: Tegra 4 (2014)**

Proprietary ISP-embedded algorithms use GPU for acceleration \(\rightarrow\) \(~10x\) speedup and cost power

**Fig: Camera architecture in current high-end mobile devices**

**Fig: Chimera: The NVIDIA computational photography arch.**

\(1^{st}\) real-time HDR, \(1^{st}\) HDR panorama, \(1^{st}\) object tracking

SOURCE: NVIDIA whitepaper, MWC ‘13
What are their limitations?

2. Current algorithmic solutions: slow on CPUs

Our target: ~100x speedup compared to software

Image registration is a computational bottleneck → needs acceleration
What have we done about it?

We propose an architecture for MFP that has a dedicated accelerator for image registration.
What are our findings?

AMETHYST shows speed-up of: **8x** over GPU and **5x** over FPGA
at a power lower by: **14x** than GPU and **3x** than FPGA

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* synthesis results for (IPD+DFE) blocks only

* assuming 60% cost due to (IPD + DFE)

* performance and power are estimated values
What are our findings? Contd...

Highlights

- State-of-the-art algorithm$^\text{§}$ (from Photosynth)
- 1st MFP engine for re-targetable applications
- Extensively configurable parallelism
- Multi-level data pipelining and interleaving
- Systolic ops w/ 2-level vector reduction

$^\text{§}$M. Brown et al., PAMI '10
Technical steps:

- Finish implementing RTL for HE and IWP modules
- Verify full-design on FPGA-based programmable SoCs (e.g., Zynq)
- Develop HW-SW co-design with ARM core towards custom SoC
- Perform physical design and post-layout validation of SoC
- Integrate silicon-proven design IP with ISP core

Stage 1: FPGA validation

Stage 2: Silicon validation

Stage 3: ISP integration