Eric S. Chung

Curriculum Vitae

Microsoft Research
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Redmond, WA 98052

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Interests

Computer architecture, cloud and datacenter architecture, deep learning, specialized computing & accelerators, FPGAs, ASICs, high-level synthesis, simulation, modeling, and design automation.

Achievements

Platform architect for Project Catapult, which pioneered the novel uses and widespread adoption of FPGAs for datacenter acceleration. Drove the pathfinding that enabled Microsoft product and research groups to harness FPGAs successfully, including achieving nearly 100% speedup of the Bing search ranking algorithm. Successes cited frequently in executive briefings and played a major factor in Microsoft's decision to incorporate FPGAs worldwide into its datacenters (millions of servers now spanning 15 continents and 5 countries). Catapult has been cited as the reason for Intel's $16.7B acquisition of Altera.

Founder of Project BrainWave, a large-scale machine learning platform harnessing FPGAs at datacenter scale. Led a team that pioneered and shipped Microsoft's first FPGA-powered DNNs into production (demoed personally to CEO Satya Nadella, reviewed positively by both Satya and Bill Gates). The BrainWave technology was demoed as an "AI Supercomputer" at Satya's IGNITE keynote in 2016 (20,000 in attendance), highlighting the ability to translate all of Wikipedia in under a tenth of a second using FPGA-powered DNNs.

Education

- **Carnegie Mellon University – Pittsburgh, PA**
  PhD in Electrical and Computer Engineering, 2004 - 2011
- **University of California Berkeley – Berkeley, CA**
  B.S. in Electrical Engineering and Computer Science, 2001 - 2004

Professional Experiences

- Senior Researcher/Research Manager, 2017-present, *Microsoft Research NeXT*
  Redmond, WA, Manager: Doug Burger
- Researcher, 2013-2017, *Microsoft Research NeXT*
  Redmond, WA, Manager: Doug Burger
- Post-doctoral Researcher, 2011-2013, *Microsoft Research SVC, Computer Architecture Group*
  Mountain View, CA, Manager: Chuck Thacker
- Graduate Student Researcher, 2004-2011, *Carnegie Mellon University, Computer Architecture Lab*
  Pittsburgh, PA, Advisor: James C. Hoe
- Research Intern, May—2008, *Microsoft Research SVC, Computer Architecture Group*
  Mountain View, CA, Manager: Chuck Thacker
- Research Assistant, 2002—2004, *Group for User Interface Research at UC Berkeley*
  Berkeley, CA, Mentors: Prof. James Landay, Prof. Jason Hong, Jimmy Lin
- Co-founder, 2008—*Meganudge Entertainment LLC,* Pittsburgh, PA
  (developed, marketed, and released a Top 25 iPhone app featured by Apple)
- Co-founder, 2003—2005, *Berkeley Innovation* – Berkeley, CA

Honors and Awards

- IEEE TCCA Young Computer Architect Award (2017)
- Young Researcher at the Heidelberg Laureate Forum (2013)
- Microsoft Research Graduate Fellowship (2009-2010)
- John and Claire Bertucci Graduate Fellowship (2011)
- Carnegie Mellon Laboratory for Computer Systems Fellowship (2004)
- Department Honors, University of California Berkeley (2004)
- National Collegiate Inventors & Innovators Alliance Advanced E-Team Award (2004)
- Eta Kappa Nu: Berkeley Mu Chapter (2002)

Paper Awards/Recognition

- 2017: "A Cloud-Scale Acceleration Architecture" (IEEE MICRO Top Picks in Computer Architecture)
- 2016: "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services" (Communications of the ACM Research Highlights).
- 2015: "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services" (IEEE MICRO Top Picks in Computer Architecture).
- 2011: "CoRAM: An In-Fabric Memory Architecture for FPGA-based Computing" (International Symposium on Field Programmable Gate Arrays 2011 Best Paper Award).

Media Highlights

- Catapult AI engine publicly demoed at Microsoft CEO Satya Nadella's keynote ("AI Supercomputer"), *IGNITE 2016*, September 26, 2016.
- (Interviewed) "Microsoft Bets Its Future on a Reprogrammable Computer Chip", September 25, 2016, *Wired Magazine*.
- (Interviewed) "Microsoft Says Programmable Chips Will Make AI Software Smarter", August 25, 2015, *MIT Technology Review.*
- "Microsoft Supercharges Bing Search With Programmable Chips", June 16, 2014, *Wired Magazine*.

Previous Research

- **CoRAM: A Scalable, Portable Memory Architecture for FPGA-based Computing (2009—2011)**
  At CMU, I led the CoRAM project, an effort to harness FPGAs for acceleration while tackling their portability and programmability challenges.
- **ProtoFlex: FPGA-based Simulation of Full-System Multiprocessors (2005—2010)**
  Lead developer of the ProtoFlex project at CMU, which demonstrated virtualized full-system simulations of multiprocessors using FPGAs. ProtoFlex pioneered *hybrid simulation* and *host interleaving* techniques, which made it practical to emulate a 16-way UltraSPARC III multiprocessor system running Oracle TPC-C on a single FPGA.
- **Specialized Hardware for Big Data (2011—2013)**
  Led the LINQits project, an effort to build composable, flexible hardware templates for accelerating data-intensive applications efficiently on mobile devices.
- **A Low-Cost Circuit-Switched Datacenter Network (2011—2013)**
  Collaborated with Chuck Thacker, Andreas Nowatyzk, Tom Rodeheffer, and Fang Yu to develop a low-cost, FPGA-based circuit-switched network for the datacenter. Developed the RTL implementation of a high-radix, 128x128 circuit-switched crossbar targeting FPGAs.

Professional Service

Conference Organization

- General Chair, International Symposium on Workload Characterization (IISWC), 2017
- Proceedings Chair, International Symposium on Computer Architecture (ISCA), 2015
- Proceedings Chair, International Symposium on Computer Architecture (ISCA), 2014
- Panel Chair, "Reconfigurable Computing in the Era of Dark Silicon", International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2013

Technical Program Committees

- International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2017, 2016, 2015, 2014, 2013, 2012
- International Symposium on Field-Programmable Gate Arrays (FPGA), 2016, 2017, 2018,
- International Symposium on Computer Architecture (ISCA), 2017 (ERC), 2018
- International Symposium on Microarchitecture (MICRO), 2017, 2018
- International Symposium on High-Performance Computer Architecture (HPCA), 2018
- International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2017
- Computer Architecture and High Performance Computing (SBAC-PAD), 2014, 2013
- Workshop on Architectures and Systems for Big Data (ASBD), 2015, 2014

Best Paper Award Committee

- International Symposium on Field-Programmable Gate Arrays (FPGA), 2016
- International Symposium on Microarchitecture (MICRO), 2012

External Reviewer

- IEEE Micro Special Issue on Big Data (IEEE MICRO), 2014
- ACM Transactions on Architecture and Code Optimization (ACM TACO), 2014
- International Symposium on High Performance Computer Architecture (HPCA), 2013
- Workshop on Intersections of Computer Architecture and Reconfigurable Logic (CARL), 2013
- International Journal of Parallel Programming (IJPP), 2014
- European Network on High Performance and Embedded Architecture and Compilation (HIPEAC)
- IEEE Transactions on Parallel and Distributed Systems (TPDS), 2013

Societies

- IEEE Computer Society
- ACM SIGARCH

Fully-Reviewed Conference and Journal Publications

1. Adrian M. Caulfield, Eric S. Chung, Andrew Putnam, Hari Angepat, Jeremy Fowers, Michael Haselman, Stephen Heil, Matt Humphrey, Puneet Kaur, Joo-Young Kim, Daniel Lo, Todd Massengill, Kalin Ovtcharov, Michael Papamichael, Lisa Woods, Sitaram Lanka, Derek Chiou, Doug Burger. "A Cloud-Scale Acceleration Architecture." *International Symposium on Microarchitecture (MICRO),* Taipei, Taiwan, October 2016. ***(IEEE MICRO Top Picks 2017)***
2. Kalin Ovtcharov, Olatunji Ruwase, Joo-Young Kim, Jeremy Fowers, Karin Strauss, Eric S. Chung. "Toward Accelerating Deep Learning at Scale Using Specialized Logic." *Hot Chips: A Symposium on High Performance Chips (HOTCHIPS)*, August 1, 2015.
3. Andrew Putnam, Adrian M Caulfield, Eric S Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Gopi Prashanth Gopal, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, Joo-Young Kim, Sitaram Lanka, James Larus, Eric Peterson, Simon Pope,

Aaron Smith, Jason Thong, Phillip Yi Xiao, Doug Burger. "A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services." *International Symposium on Computer Architecture (ISCA),* Minneapolis, MN, June 2014. ***(IEEE MICRO Top Picks 2015, CACM Highlights 2016)***

4. Eric S. Chung, John D. Davis, Jaewon Lee. "LINQits: Big Data on Little Clients." *International Symposium on Computer Architecture (ISCA)*, Tel-Aviv, Israel, June 2013.
5. Eric S. Chung, Michael K. Papamichael. "ShrinkWrap: Compiler-Enabled Optimization and Customization of Soft Memory Interconnects." *International Symposium on Field-Programmable Custom Computing Machines (FCCM),* Seattle, WA, April 2013.
6. Eric S. Chung, Michael K. Papamichael, Gabriel Weisz, James C. Hoe, Ken Mai. "Prototype and Evaluation of the CoRAM Memory Architecture for FPGA-Based Computing." *International Symposium on Field-Programmable Gate Arrays (FPGA),* Monterey, CA, Feb 2012.
7. Srinidhi Kestur, John D. Davis, Eric S. Chung. "Towards a Universal FPGA Matrix-Vector Multiplication Architecture." *International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, Toronto, Canada, Apr 2012.
8. Eric S. Chung, James C. Hoe, Ken Mai. "CoRAM: An In-Fabric Memory Architecture for FPGA-based Computing." *International Symposium on Field-Programmable Gate Arrays (FPGA),* Monterey, CA, Feb 2011. **(FPGA'11 Best Paper Award)**
9. Eric S. Chung, Peter A. Milder, James C. Hoe, Ken Mai. "Single-Chip Heterogeneous Computing: Does the Future Include Custom Logic, FPGAs, and GPGPUs?" *International Symposium on Microarchitecture (MICRO),* Atlanta, GA, Dec 2010.
10. Eric S. Chung, James C. Hoe. "High-Level Design and Validation of the BlueSPARC Multithreaded Processor." *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol.29, no.10,* Oct 2010.
11. Eric S. Chung, Michael K. Papamichael, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai. "ProtoFlex: Towards Scalable, Full-System Multiprocessor Simulations Using FPGAs." *ACM Transactions on Reconfigurable Technology and Systems (TRETS), Volume 2, Issue 2,* Jun 2009.
12. Eric S. Chung, James C. Hoe. "Implementing a High-performance Multithreaded Microprocessor: A Case Study in High-level Design and Validation." *Formal Methods and Models for Codesign (MEMOCODE),* Cambridge, MA, Jul 2009.
13. Eric S. Chung, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai. "A Complexity-Effective Architecture for Accelerating Full-System Multiprocessor Simulations using FPGAs." *International Symposium on Field-Programmable Gate Arrays (FPGA),* Monterey, CA, Feb 2008.
14. Brian T. Gold, Jared C. Smolens, Jangwoo Kim, Eric S. Chung, Vasileios Liaskovitis, Eriko Nurvitadhi, Babak Falsafi, James C. Hoe, Andreas G. Nowatzyk. "TRUSS: Reliable, Scalable Server Architecture." *IEEE Micro, Special Issue on Reliability-Aware Microarchitectures,* Nov-Dec 2005.
15. Eric S. Chung, Jason I. Hong, James Lin, Madhu K. Prabaker, James A. Landay, Alan L. Liu. "Design Patterns for Ubiquitous Computing." *Designing Interactive Systems (DIS),* Cambridge, MA, Aug, 2004.

Other Publications

Technical Reports

16. Kalin Ovtcharov, Olatunji Ruwase, Joo-Young Kim, Jeremy Fowers, Karin Strauss, Eric S. Chung, "Accelerating Deep Convolutional Neural Networks Using Specialized Hardware". February 22, 2015.
17. Eric S. Chung, Andreas Nowatzyk, Tom Rodeheffer, Chuck Thacker, Fang Yu. "AN3: A Low-Cost, Circuit-Switched Datacenter Network." MSR-TR-2014-35, Mar 2014.
18. John D. Davis, Eric S. Chung. "SpMV: A Memory-Bound Application on the GPU Stuck Between a Rock and a Hard Place." *MSR-TR-2012-95*, Sep 2012.

19. Jangwoo Kim, Eriko Nurvitadhi, Eric S. Chung. "Opportunity of Hardware-based Optimistic Concurrency in OLTP." *Selected Project Reports from Advanced OS & Distributed Systems, Spring 2005. Technical report CMU-CS-05-138.*

Workshops and Posters

20. Eric S. Chung, Michael K. Papamichael. "Towards Automatic Customization of Interconnect and Memory in the CoRAM Abstraction (poster)." *International Symposium on Field Programmable Gate Arrays (FPGA)*, Monterey CA, Feb 2013.
21. Eric S. Chung, John D. Davis, Srinidhi Kestur. "An FPGA Drop-In Replacement for Universal Matrix-Vector Multiplication." *Workshop on the Intersections of Computer Architecture and Reconfigurable Logic (CARL)*, Portland, Oregon, Jun, 2012.
22. Eric S. Chung, James C. Hoe, Ken Mai. "Connected RAM: An In-Fabric Memory Abstraction for FPGA-Based Computing." *Workshop on the Intersections of Computer Architecture and Reconfigurable Logic (CARL),* Atlanta, GA, Dec, 2010.
23. Eric S. Chung, Michael K. Papamichael, James C. Hoe, Babak Falsafi, Ken Mai. "The Open-Source ProtoFlex Simulator (poster)." *Research Accelerator for Multiple Processors (RAMP),* Santa Cruz, CA, Jan 2010.
24. Eric S. Chung, Michael K. Papamichael, James C. Hoe, Babak Falsafi, Ken Mai. "ProtoFlex: Towards Scalable, Full-System Multiprocessor Simulations Using FPGAs (poster)." *Center for Circuit and System Solutions (C2S2) Annual Review*, 2009.
25. Michael K. Papamichael, Eric S. Chung, James C. Hoe, Babak Falsafi, Ken Mai. "ProtoFlex: Complexity-Effective FPGA-Accelerated Instrumentation (poster)." *Research Accelerator for Multiple Processors (RAMP Retreat)*, Palo Alto, CA, Aug 2008.
26. Eric S. Chung, Michael K. Papamichael, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai. "An MP Architectural Exploration Vehicle Using Complexity-Effective FPGA-accelerated Simulation (poster)." *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS),* Seattle, WA, March 2, 2008.
27. Eric S. Chung, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai. "Virtualized Full-System Emulation of Multiprocessors using FPGAs." *Workshop on Architecture Research Prototyping (WARP)*, June 2007.
28. Eric S. Chung, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, Ken Mai. "ProtoFlex: FPGA-Accelerated Hybrid Functional Simulator." *Workshop on NSF Next Generation Software Program (NSFNGS)*, Mar 2007.
29. Eric S. Chung, James C. Hoe, Babak Falsafi. "ProtoFlex: Co-Simulation for Component-wise FPGA Emulator Development." *Workshop on Architecture Research using FPGA Platforms (WARFP)*, Austin, TX, Feb 2006.

Patents

25. Deep Neural network partitioning on servers. US Patent App. 14/754,384.
26. Server systems with hardware accelerators including stacked memory. US Patent App. 14/754,295.
27. Deep neural network processing on hardware accelerators with stacked memory. US Patent App. 14/754,344.
28. Convolutional neural networks on hardware accelerators. US Patent App. 14/754,367.
29. Machine learning classification on hardware accelerators with stacked memory. US Patent App. 14/754,323.
30. In-line network accelerator. US Patent App. 14/752,734.
31. Lightweight transport protocol. US Patent App. 14/752,713.
32. Locally restoring functionality at acceleration components. US Patent App. 14/752,802.
33. Restoring service acceleration. US Patent App. 14/752,782.
34. Reconfiguring an acceleration component among interconnected acceleration components. US Patent App. 14/752,793.

35. Protecting communications with hardware accelerators for increased workflow security. US Patent App. 14/742,702.
36. Independently networkable hardware accelerators for increased workflow optimization. US Patent App. 14/735,108.
37. Providing Services in a System having a Hardware Acceleration Plane and a Software Plane. US Patent App. 14/717,721.
38. Implementing a Service Using Plural Acceleration Components. US Patent App. 14/717,788.
39. Dynamic power routing to hardware accelerators. US Patent App. 14/682,088.
40. Hardware acceleration for query operators. US Patent App. 13/900,537.
41. Universal FPGA matrix-vector multiplication architecture. US Patent 9,317,482.

Books

42. Hari Angepat, Derek Chiou, Eric S. Chung, James C. Hoe. "FPGA-Accelerated Simulation of Computer Systems", *Morgan & Claypool Publishers: Synthesis Lectures on Computer Architecture*, 2015.

Talks

43. "Accelerating Persistent Neural Networks at Datacenter Scale", Symposium on High Performance Chips (Hot Chips), August 22, 2017.
44. (Invited talk) "Deep Learning in the Enhanced Cloud", International Symposium on Physical Design (ISPD), March 20, 2017.
45. (Invited talk) "Deep Learning in the Enhanced Cloud", *SILO invited speaker, University of Wisconsin-Madison*, November 9, 2016.
46. (Invited talk) "Agile Co-Design for a Reconfigurable Datacenter", *Workshop at International Symposium on Field-Programmable Gate Arrays (FPGA)*, February 21, 2016.
47. (Invited talk) "Accelerating Artificial Intelligence at Cloud Scale", *Frontiers in Neuromorphics Workshop*, April 14-15, 2016.
48. (Invited talk) "Toward Accelerating Deep Learning at Scale Using Specialized Logic", *Hardware and Algorithms for Learning-on-a-Chip (HALO),* November 4, 2015.
49. (Invited talk) "Toward Accelerating Deep Learning at Scale Using Specialized Hardware in the Datacenter", *CALCM seminar, Carnegie Mellon University*, October 20, 2015.
50. "Toward Accelerating Deep Learning at Scale Using Specialized Logic", *Hot Chips: A Symposium on High Performance Chips (HOT CHIPS)*, August 25, 2015.
51. (Invited talk) "Accelerating Deep Convolutional Neural Networks Using Specialized Hardware in the Datacenter", *Workshop on Computer Architecture for Machine Learning (CAMEL)*, June 14, 2015.
52. "LINQits: Big Data on Little Clients", *International Symposium on Computer Architecture (ISCA)*, June 26, 2013.
53. (Invited talk) "Towards Logic Specialization for the Masses", EcoCloud Annual Event, May 31, 2013.
54. Invited Talk on CoRAM at Microsemi, Inc., San Jose, CA, March 15, 2012.
55. Invited Talk on CoRAM at Xilinx, Inc., Campbell, CA, January 20, 2012.
56. Invited Talk on CoRAM at Altera, Inc., San Jose, CA, March 3, 2011.
57. "Prototype and Evaluation of the CoRAM Memory Architecture for FPGA-Based Computing", *International Symposium on Field-Programmable Gate Arrays (FPGA),* Monterey, CA, February 23, 2012.
58. "CoRAM: An In-Fabric Memory Architecture for FPGA-Based Computing." *International Symposium on Field-Programmable Gate Arrays (FPGA)*, Monterey, CA, February 28, 2011.
59. "Single-Chip Heterogeneous Computing: Does the Future Include Custom Logic, FPGAs, and GPGPUs?" *International Symposium on Microarchitecture (MICRO)*, Atlanta, GA, December 6, 2010.
60. "CoRAM: An In-Fabric Memory Abstraction for FPGA-Based Computing." *Workshop on the Intersections of Computer Architecture and Reconfigurable Logic (CARL),* Atlanta, GA, December 5, 2010.

61. "Implementing a High-performance Multithreaded Microprocessor: A Case Study in High-level Design and Validation." *Formal Methods and Models for Codesign (MEMOCODE),* Cambridge, MA, July 14, 2009.
62. "Open Source Protoflex Simulator." *Research Accelerator for Multiple Processors (RAMP retreat)*, Austin, TX, June 25, 2009.
63. "A Complexity-Effective Architecture for Accelerating Full-System Multiprocessor Simulations Using FPGAs." *International Symposium on Field-Programmable Gate Arrays (FPGA),* Monterey, CA, Feb, 2008.
64. "Usability Challenges for RAMP2." *RAMP retreat*, Berkeley, CA, January 15, 2009.
65. "A Complexity-Effective Architecture for Accelerating Full-System Multiprocessor Simulations Using FPGAs." *Invited Talk at SUN Microsystems*, Santa Clara, CA, January 17, 2008
66. "ProtoFlex Status Update and Design Experiences." *RAMP retreat*, Berkeley, CA, January 17, 2008.
67. "Accelerating Architectural-Level Full-System Simulations Using FPGAs." *Invited talk at Microsoft Research*, Redmond, CA, October 24, 2007.
68. "Architectural Emulation on FPGAs Made Easy with Bluespec." *Bluespec Workshop*, MA, Aug, 2007.
69. "Virtualized Full-System Emulation of Multiprocessors using FPGAs." *Workshop on Architecture Research Prototyping (WARP)*, June 9, 2007.
70. "Protoflex: An FPGA-Accelerated Hybrid Functional Simulator." *RAMP retreat*, Berkeley, CA, Jan, 2007.
71. "Combining Simulators and FPGAs: An Out-of-Body Experience." *RAMP retreat*, Boston, MA, Jun, 2006.
72. "ProtoFlex: Co-Simulation for Component-wise FPGA Emulator Development." *Workshop on Architecture Research using FPGA Platforms (WARFP)*, Austin, TX, February 12, 2006.

Tutorials at Conferences

73. Eric S. Chung, Michael K. Papamichael, Gabriel Weisz. "Cross-Platform FPGA Accelerator Development Using the CoRAM Virtual Architecture and the CONNECT Network-on-Chip Generator." *Tutorial at International Symposium on Field Programmable Gate Arrays (FPGA)*, February 11, 2013.
74. Eric S. Chung, Michael K. Papamichael, Gabriel Weisz. "Cross-Platform FPGA Accelerator Development Using the CoRAM Virtual Architecture and the CONNECT Network-on-Chip Generator." *Tutorial at International Symposium on Microarchitecture (MICRO)*, December 6, 2012.
75. Derek Chiou, Eric S. Chung, Michael K. Papamichael, Hari Angepat, Angshuman Parashar, Zhangi Tan. "RAMP Simulator Tutorial: Protoflex, FAST, HAsim, and RAMP-Gold." *Tutorial at International Symposium on Performance Analysis of Systems and Software (ISPASS)*, Mar, 2010.
76. Eric S. Chung, Mike Ferdman, and Michael K. Papamichael. "SimFlex and ProtoFlex." *Tutorial at International Symposium on Microarchitecture (MICRO)*, December 12, 2009.
77. Eric S. Chung, Michael K. Papamichael. "ProtoFlex: An Architectural Exploration Vehicle using FPGA-Accelerated, Full-System Multiprocessor Simulation." *Tutorial at International Symposium on Workload Characterization (2009)*, October 4, 2008.
78. Eric S. Chung, Michael K. Papamichael. "ProtoFlex Tutorial: Full-System MP Simulations Using FPGAs." *Tutorial at International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2, 2008.
79. Eric S. Chung, Eriko Nurvitadhi, James C. Hoe, Babak Falsafi, and Ken Mai. "RAMP tutorial: ProtoFlex." *Tutorial at International Symposium on Computer Architecture (ISCA)*, San Diego, CA, June 10, 2007.

Grants

80. CCF-SHF: Rethinking the Architecture of FPGAs as First-Class Computing Devices (NSF; CCF-1012851; J. Hoe—PI, K. Mai—Co-PI; $1,000,000, 2010-2014)
81. CPA-CSA: Accelerating Architectural-level, Full-system Multiprocessor Simulations Using FPGAs (NSF; CCF-0811702; J. Hoe—PI, $314,000, 2008-2011)

Supervision

Interns

- Blaise Tine, Georgia Institute of Technology
- Jialiang Zhang, University of Wisconsin-Madison
- Bita Rouhani, University of California San Diego
- Ming Liu, Massachusetts Institute of Technology
- Pareesa Golnari, Princeton University
- Divya Mahajan, Georgia Tech University
- Jongse Park, Georgia Tech University
- Stuart Byma, EPFL
- John Demme, Columbia University
- Shenghsun Cho, Stonybrook University
- Dan Zhang, University of Texas at Austin
- Samuel Grossman, Stanford University
- Daniel Barowy, University of Massachusetts Amherst
- Jaewon Lee, Pohang University of Science and Technology
- Maysam Lavasani, University of Texas at Austin
- Srinidhi Kestur, University of Pennsylvania
- Taylor Womak, Carnegie Mellon University
- Sriteja Tangeda, Carnegie Mellon University

Thesis Committees

- Maysam Lavasani, University of Texas at Austin

Teaching

- 18-240: Fundamentals of Computer Engineering at CMU with Prof. James Hoe (2006, TA rating: 4.5/5.0)
- 18-741: Advanced Computer Architecture at CMU with Prof. James Hoe (2005, TA rating: 4.7/5.0)
- CS150: Design Techniques for Digital Systems at UCB with Prof. Randy Katz (2004, TA rating: 4.1/5.0)
- EE42: Intro to Digital Electronics at UCB with Prof. Andrew Neureuther (2003, TA rating: 4.8/5.0)

Personal

- US citizen
- Languages: English, Mandarin